REMARKS

Reference characters 901, 109, and 1215 in Figures 9, 10, and 11 that were not mentioned in the description are now amended in paragraphs 29, 30, and 34.

The error of antecedent basis in claim 13 has been amended.

Office Action Rejections Summary

Claim 1 has been rejected under 35 U.S.C. 102(e) as being anticipated by **Ostrom** of US-2002/0046354 (hereinafter "**Ostrom**").

Claims 22, 24 have been rejected under 35 U.S.C. 102(b) as being anticipated by **Nicol** of US Patent 6,141,762 (hereinafter "**Nicol**").

Claims 2-3, 5, 7-10, 12, 14-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** as applied above and to **Isaac** of US Patent 6,327,663 (hereinafter "**Isaac**").

Claims 4, 6, 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above, and in view of **Wright** et al. of US Patent 5,774,736 (hereinafter "**Wright**")

Claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above, and in view **Kanouda** et al. of US Patent.

Claim 16-21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above, and further in view of **Kanouda** as applied above, and **Maitra** of US Patent 5,623,647 (hereinafter "**Maitra**").

Status of Claims

Claims 1-22 and 24 remain pending in the application. Claims 1, 8, 16, and 22 have been amended. Claim 23 has been cancelled. No new matter has been added.

Claim Rejections – 35 U.S.C. § 102

Claim 1 has been rejected under 35 U.S.C. 102(e) as being anticipated by **Ostrom**. **Ostrom** teaches a device to detect when a transient event occurs for providing power to suppress transient load demands (Abstract). The device includes one or more power regulators and a sense circuit that is coupled to a load. The power regulator may regulate voltage or current in response to a rate of change in current or a rate of change in voltage as demanded by the load (paragraph 0010). Nothing in **Ostrom** teaches a controller that responds to a change in power level and is used to prevent power droop.

In contrast, applicant's disclosed voltage controller functions in response to inputs such as current, voltage, frequency and power supply input (paragraph 0035) and is used to boost voltage to a processor to compensate for a voltage droop (paragraphs 0007-0008). As such, applicant submits that claim1 is not anticipated by **Ostrom** under 35 U.S.C. §102(e) and respectfully request the withdrawal of the rejection of that claim.

Claims 22, 24 have been rejected under 35 U.S.C. 102(b) as being anticipated by **Nicol**. **Nicol** teaches a method and an apparatus to minimize overall power consumption of a multi-processor chip by allocating tasks to individual processors to equalize processing load among the chips, thereby lowering clock frequency on the chip to as low a level as possible and thus reducing the supply voltage (Abstract). Claim 22 has been amended to include the allowable subject matter of claim 23, and thus claim 22 is now allowable.

Claim Rejections – 35 U.S.C. § 103

Claims 2-3, 5, 7-10, 12, and 14-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** as applied above and to **Isaac**. **Ostrom** is described

above and nothing in **Ostrom** discloses a voltage controller that responds to a change in power and is used to prevent power droop.

Isaac teaches a method and system for preventing electronic overstress during powering up a processor with voltage detection capability (Abstract). The system includes a detection mechanism or over stress protection system (OSPS) coupled, a processor and a power supply. The OSPS detects the voltage requirements of the processor through logic signals thereby adjusting the power supply of the motherboard to the processor voltage requirement (Abstract). The OSPS includes a voltage detection unit and a voltage control unit. The former is coupled to a processor and the later is coupled to a voltage regulating circuitry of power supply (Col. 5 lines 28-32). The OSPS operates during the powering up phase of the processor and performs its functions prior to the actual powering up of the processor (Col. 5, lines 47-58). The OSPS is designed to prevent the power supplied to the processor from becoming too high and overloading the processor. Nothing in **Isaac** teaches that the power controller functions to increase power to prevent a power droop or a voltage droop. Thus, **Isaac** fails to cure the deficiency of **Ostrom**.

Applicant submits that there is no motivation to combine **Ostrom** and **Isaac**. **Isaac**'s invention, an over stress protection system (OSPS), includes a voltage detection unit and a voltage control unit coupled to the power supply and the processor, is used to prevent overstress of the system by controlling the voltage supply to the processor and essentially functions prior to actual powering up of the processor (Col. 5, lines 52-59). **Ostrom**'s invention is aimed to respond to slow or fast transient events through the use of one or two power regulators to suppress transient load demands through the detection of current or voltage load. Neither reference suggests the detection of load changes as a function of voltage, current, frequency, power supply or a combination thereof, and while

both references were designed to prevent stress or overload to the circuit, neither was designed with the opposite effect of boosting power to the circuit to prevent power droop.

Applicant submits that **Ostrom** and **Isaac** do not teach or suggest a combination with each other. Claims 2, 3, 5, 7, 9, 10, 12, and 14-15 either directly or indirectly depend on the amended independent claims 1 and 8 and thus they are allowable. As such, applicant respectfully submits that claims 2, 3, 5, 7-10, 12, and 14-15 are not unpatentable over **Ostrom** in view of **Isaac** and requests the withdrawal of the rejection of the claims.

Claims 4, 6, and 13 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above, and in view of **Wright**. As described above, neither **Ostrom** nor **Isaac** cures the deficiency of each other nor do they teach or suggest a combination with each other.

Wright teaches a fault tolerant system for providing power to a multiple central processing unit computer system through the use of multiple DC-DC converters (Abstract). Three DC-DC converters are used to power two central processing units (CPU). Each DC-DC converter has an output voltage level selectable through a voltage identification signal. A voltage reference circuit functions as a voltage regulator which furnishes the reference voltage protection circuit, which in turn, determines whether the output of the DC-DC converters is above a maximum output voltage or below a minimum output voltage level. A reference selection circuit combining with the voltage reference circuit is used to adjust the reference voltage level according to the desired output voltage level of the DC-DC converter as indicated by the voltage identification signal (Col. 10, lines 59-65). If the voltage identification signals match, identification logic couples the power planes together, but if only one converter is available to power the two central processing units, a stop clock logic circuit alternatively places the central processing units

and only a single converter has to fully power one CPU at any one time (Abstract). As such, **Wright** fails to cure the deficiency of **Ostrom** and **Isaac.**

Applicant submits that there is no motivation to combine **Ostrom**, **Isaac** and **Wright**. As described above, neither **Ostrom** nor **Isaac** teaches or suggests a combination with each other. **Wright**'s disclosure relates to a fault tolerant system for providing power to a multiple central processing unit computer system. Similar to **Isaac**, **Wright**'s disclosure detects voltage directly. **Wright**'s disclosure also includes multiple power regulators (DC-DC converters) and CPUs and relates to providing and distributing power among the CPUs to maximize power efficiency such that the converter and CPUs do not have to shut down while preserving functionality of each CPU (Col. 2, lines 34-41). **Wright** utilizes a voltage comparator to compare voltage identification signals to activate a switch circuit for coupling different power planes together to furnish redundant power to the computer system. Nothing in **Wright** discloses or suggests that its power level changes to prevent power droop of the circuit.

Applicant submits that since **Wright** neither cures nor suggests or teaches a cure for the deficiencies of **Ostrom** and **Isaac**, there is no motivation to combine the three references. Claims 4, 6, and 13 either directly or indirectly depend on amended independent claims 1 and 8 and thus they are allowable. As such, applicant respectfully submits that claims 4, 6, and 13 are not unpatentable over **Ostrom**, in view of **Isaac** and **Wright** and respectfully requests the withdrawal of the rejection of the claims.

Claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above, and in view of **Kanouda**. As described above, **Ostrom** and **Isaac** fails to cure the deficiency of each other and do not suggest or teach a combination with each other.

Kanouda teaches a voltage regulator module that includes a power supply circuit for supplying power to an integrated circuit. The power supply circuit includes semiconductor switching devices driven by a drive circuit and a double layer capacitor for charge storage to smooth the output of the power supply circuit (Abstract). The power required by the CPU is determined by the increase of computation processing contents of the CPU indicated by an increase in computation processing contents (col 7, lines 24-25). In this system, it is not necessary to dispose a power supply for supplying power to the CPU close by the CPU package, but rather, power is supplied by the double layer capacitor. Nothing in **Kanouda** teaches or discloses that voltage level is increased as a function of voltage, current, frequency, power supply or a combination thereof, thus it fails to cure the deficiency of **Ostrom** and **Isaac**.

Applicant submits that there is no motivation to combine **Kanouda** in view of **Ostrom** and **Isaac**. **Kanouda**'s voltage regulator module detects current changes and generates power or electric potential from a double layer capacitor charge source without using an additional power supply.

Applicant submits that **Kanouda**, **Ostrom,** and **Isaac** do not suggest or teach a combination with each other. Amended independent claim 8 contains the limitation "to prevent voltage droop." Claim 11 indirectly depends on independent claim 8 and so includes the limitation. Thus applicant respectfully submits that claim 11 is not unpatentable under 35 U.S.C. 103(a) over **Ostrom** in view of **Isaac** and **Kanouda** and requests withdrawal of the rejection of the claim.

Claims 16 – 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over **Ostrom** and **Isaac** as applied above in view of **Kanouda**, and further in view of **Maitra**. As described above, **Ostrom**, **Isaac**, and **Kanouda** fail to cure the deficiency of each other and do not teach or suggest a combination with each other.

Maitra teaches an apparatus that adjusts the CPU clock of the microprocessor to meet the computing requirement of applications run by the microprocessor (Abstract). This apparatus is designed to reduce power consumption and heat dissipation of the microprocessor. To optimize power efficiency, the apparatus manages the operating speed of the microprocessor by determining the application that is run in the present time quantum, determining the application's computing requirement, and adjusting the microprocessor's operation speed to meet the requirement (Abstract). Nothing in **Maitra** teaches or discloses increasing the voltage level for a predetermined amount of time to prevent power droop in response to the determining, according to the compute load, of the power level needed.

Applicant submits that there is no motivation to combine **Ostrom**, **Isaac**, **Kanouda**, and **Maitra**. **Maitra**'s disclosure is designed to reduce power consumption and heat dissipation of the microprocessor by managing the operating speed of a microprocessor by determining the applicant's computing requirement and adjusting the microprocessor's operation speed to meet demand. **Maitra** determines the power consumption and adjusts the operating speed by comparing the application from the computer's operating system's task scheduler against a bench-mark evaluator such that the computing requirement of the process is determined and so that the clock speed of the microprocessor is adjusted to meet the computing requirement of the process (Col. 2, lines 43-52). **Maitra** was designed to reduce the power consumption and heat dissipation, which means reducing unnecessary current or voltage supplied to the circuit. On the contrary, applicant's invention anticipates changes in compute load levels and increases the voltage level for a predetermined period of time to prevent a power droop in response to the determining, according to the compute load, the power level needed.

Thus, Maitra neither cures the deficiency of **Ostrom**, **Isaac**, and **Kanouda**, nor suggests any reason for combination.

Applicant submits that **Maitra, Kanouda**, **Ostrom,** and **Isaac** do not suggest or teach a combination with each other. Thus applicant respectfully submits that claims 16-21 are not unpatentable under 35 U.S.C. 103(a) over **Ostrom** and **Isaac** in view of **Kanouda** and **Maitra** and requests withdrawal of the rejection of the claims.

In conclusion, applicant respectfully submits that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome. If the allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact the undersigned at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02–2666.

Respectfully submitted,
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